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10/625,285	07/22/2003	Peter R. Munguia	42P16384	7500

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,285	MUNGUIA ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-33 and 35-48* is/are rejected.

7)☒ Claim(s) *34 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-49 have been presented for examination in this application. In response to the last office action, claims 1-23 have been canceled. Claims 24-49 have been amended. The specification have been amended in the amendments filed on 2/2/07. As the result, claims 24-49 are now pending in this application.

Applicant's responses/amendments filed on 3/19/07 3/16/07 and 2/2/07 have been fully considered but they are not persuasive, Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the amendments

Claims 24-33,35-48 are rejected.

Claims 34,49 are objected to.

Claim Objections

Following claim(s) are objected to because of the following informalities:

As in claim 37, the recitation of the phrase "the single boot device" at lines 2-3 lacks antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-33,35-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over William et al (US 6199151).

As in claim 24, the claim recites an apparatus comprising: a controller, to generate, before controller initialization during boot, reset, or other pre-configuration state of the apparatus,

an unencoded chip select word in response to a default unencoded chip select mode,

an encoded chip select word in response to a default encoded chip select mode; and

wherein the encoded chip select word and the unencoded chip select word select the same boot device.

William discloses a method and apparatus to provide chip selects in either encoded or unencoded words to address any memory devices. William discloses a computer system (corresponding to the claim's apparatus) comprising a controller (William's Fig 1: #12 subsystem controller). William's controller further comprises address translation elements (William's Fig 4, TLB table, address decode logic, chip select logic) that capable of providing the address lines and chip select lines to address any memory devices. The chip select word can be either an unencoded chip select word (William's Fig 3, CS: bits 8-1), or encoded chip select word (William's Fig 3: CS bits 2-0). Both unencoded chip select word and encoded chip select word select the same memory device, for example, in Fig 3, values "00000010" and "001" points to the same memory device (William's column 6, lines 33-50). William clearly teaches the need to

quickly provide addresses, and chip select signals to memory devices and thereby improve the performance of the overall system. In this instance, William teaches a novel approach that is the controller itself with its associating logic can quickly handle/provide chip select values in both encoded and unencode forms and quickly provide individual chip select lines to memory devices (Williamn's column 1 lines 37-46, column 2 lines 6-15, column 2, lines 20-25 quick providing of chip select signal to memory device reduce the overall time to select data in a row of memory device). Although William does not expressly discloses that the memory device stores the code to initializing the system. However, it's well known in the art that memory devices are used to stored variety of codes including boot code, initializing code, operating system code, application code. Thus William's controller is clearly intent to provide quick chip select lines to any memory devices in any period of time and thereby further improve the performance of the overall system. William further discloses the chip select is provided by using either the encoded chip select or the unencoded chip select (see William's Fig 3, column 5 line 59 to column 6 line 7, various encoded schemes can be implemented). Thus obviously, the choice of encoding chip select or unencoding chip select is configured by setting a value into a "mode" register in the controller (for example, the mode register configured/setting with value 0 for selecting the unencoding chip select, and the mode register configured/setting with value 1 for selecting the encoded chip select, William's column 5 lines 49-52 discloses several configuration registers for such configuration information in the system). At power up time, the registers in the system are cleared such that the system starts with an initial state. The registers are cleared for example, by well-known mechanism in the art, using the reset signal at the power-up time. Thus the

"mode" register is cleared (by reset signal) with value zero, **before** the BIOS code is read, to select the unencoded chip select and therefore configured to generate the unencoded chip select **before** the BIOS code is read in from a non-volatile device and initializing the controller or the system.

The BIOS code as known in the art comprises several modules of information representing critical commands/data such as system configuration information, operating code for the system, being stored in storage elements of non-volatile memory devices. The BIOS code is loaded into the system and executing in a bootstrap manner. For example, the first information module stored in a first boot device having the configuration information for the system must be loaded first, before loading other information modules such as operating system. Thus it's obviously that the configuration information that indicates the state of the system, such as chip selection mode being used in the system, must be maintained in the non-volatile device, such as the first boot device, and loaded into the system before loading other information modules such as operating system.

As in claim 25, the claim recites wherein the controller comprises a memory controller

to generate the encoded chip select word and the unencoded chip select word. The claim rejected based on the same rationale as of claim 24. William's Fig 1: #12 discloses subsystem controller corresponds to the claim's memory controller to generate the encoded chip select word and the unencoded chip select word (William's column 6 lines 13-26).

As in claim 26, the claim recites wherein the memory controller comprises an address

decoder to generate the encoded chip select word and the unencoded chip select word (William's column 6 lines 18-25, logic to generate encoded row values to be stored in TLB).

As in claim 27, the claim recites wherein controller initialization comprises configuration of the controller to operate in an encoded chip select mode or in an unencoded chip select mode (William's column 6 lines 1-6 discloses the controller capable of being configured to operated in encoded chip select mode and/or in unencoded chip select mode).

As in claim 28, the claim recites wherein the controller comprises a configuration store

to store configuration data to configure the controller to operate in an encoded chip select mode

or in an unencoded chip select mode. The claim rejected based on the same rationale as of claim 27. William's column 6 lines 1-6 teaches the controller capable being configured to operated in encoded chip select mode and/or in unencoded chip select mode, therefore inherently the configuration information must be stored in some storage elements in order to convey to the controller the modes in which the controller must be operated on.

As in claim 29, the claim recites wherein the selected boot device comprises a memory device. It's a well known in the art that a memory device is used to boot the system.

As in claim 30, the claim recites wherein the unencoded chip select word comprises a first bit pattern and the encoded chip select word comprises a second bit pattern and the first bit pattern includes the second bit pattern William's Fig 4 discloses the unencoded chip select word/first bit pattern includes the encoded chip select word/second bit pattern. For example in Fig 4 row 2, the CS 8-1 bit pattern "00000010" includes the CS 2-0 bit pattern "001".

As in claim 31, the claim recites wherein the lowest order bits of the first bit pattern include the second bit pattern. William does not expressly disclose the claim's limitation. However William clearly suggests the controller capable and intent to provide with any encoded bit pattern, any sequential binary values (see William's column 6 lines 2-6).

As in claim 32, the claim recites wherein the controller to generate the encoded chip select word and the unencoded chip select word in response to an address for a boot code nub and the selected boot device comprises the boot code nub. The claim rejected based on the same rationale as of claim 24. William's column 5 lines 35-60 discloses the controller having configuration registers to store addresses of different memory devices being used during different period of time, therefore, it is understood that these configuration registers including addresses of memory devices for storing any data including application code, operation system code, boot code etc.. Furthermore, these configuration registers can be easily programmed with pre-determined values at start up time whether by BIOS code (as an example disclosed in William's column 5 lines 40-47) or some well known techniques in the art, for example pre-setting registers values by

using tie up/down resistors, read only registers or by scanning in pre-determine values at start up time.

As in claim 33, the claim recites wherein the controller, to generate the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one active chip select bit that corresponds to a predetermined chip-select line used to select the boot device; and the controller to generate the encoded chip select word for the address such that the

encoded chip select word comprises exactly one active chip select bit that corresponds to the

predetermined chip-select line. The claim rejected based on the same rationale as of claim 32. William's column 6 lines 40-50 disclose an individual physical chip select line CS1 to CS8 is corresponding to the encoded chip select and the unencoded chip select. William's Fig 4 row 2 further discloses one active bit of the unecoded chip select corresponds to one active bit of the encoded chip select.

As in claim 35, the claim recites wherein the encoded chip select word is generated according to an encoding scheme to assign numbers to the boot devices, the numbers to range from one to a number greater than one. The claim rejected based on the same rationale as of claim 32. William's column 5 lines 35- discloses of using configuration registers that can map address of any code stored to any memory device, wherein the number of devices to store code can be more that one (William's Fig 1; 15).

As in claim 36, the claim recites wherein the encoded chip select word is to encode the number one (see William's Fig 3 row 1, encoding the number one "00000001").

As in claim 37, the claim recites wherein the controller, in response to an address for a boot code nub that does not map to the boot device, converts the address to an address that does map to the boot device. The claim rejected based on the same rationale as of claim 32. William's column 5 lines 35-56 further discloses by matching address with the configuration registers, one can easily determine the address corresponding to a particular device. For example, if the address does not match address range in a first device, the address is further compared and if it matches address range of the second device, the address is converted to the physical address and chip select of the second device.

Claim 38 is rejected based on the same rationale as of claim 24. William's column 6 lines 1-6 further disclose the chip select word can be figured and used with any encoding schemes. That is the appraratus and controller can be easily configured to generate either unecoded chip select or encoding chip select by setting the "mode register". Regarding the boot code nub aspect of the claim. As discussed in the rationale of claim 24, the BIOS code comprises several information modules, including the information module to configure the system such as chip selection mode being used in the system (corresponding to the claim's boot nub code), which must be stored in the first boot device, and loaded into the system first before loading other information modules such as the operating system.

As in claim 39, the claim recites wherein the device storing the boot code nub is coupled to the apparatus via a predetermined chip select line, each of the other devices of the plurality of devices is coupled to the apparatus via a separate chip select line; and wherein the apparatus activates the predetermined chip select line coupled to the device

storing the boot code nub, regardless of whether the chip select word is encoded or unencoded. William's Fig 2, column 6 lines 35-50 discloses the memory device (Fig 2: #16A) is coupled to a predetermined chip select lines CS1, and the memory device (Fig 2: #17A) is coupled to a predetermined chip select lines CS2. Furthermore, it's well known in the art that the memory devices are used to store any codes (operating system, BIOS, boot code, application code). William's Fig 3 row 2 discloses both unencoded chip select and encoded chip select points to the same physical chip select line.

As in claim 40, the claim recites comprising a chip select decoder coupled to the apparatus and coupled to each of the devices of the plurality of devices via a separate chip select line, wherein, the chip decoder activates the chip select line of the device with the boot code nub in response to receiving the chip select word, regardless of whether the chip select word is encoded or unencoded. The claim rejected based on the same rationale as of claim 39. Furthermore, in order to generate the physical chip select from encoded chip select and unencoded chip select as showed in William's Fig 3, inherently a chip select decoding logic must be employed.

As in claim 41, the claim recites generating on an apparatus, in response to an address for the boot code nub and during boot, reset, or other pre-configuration state of the apparatus, a chip select word that, if the apparatus is in a default unencoded chip select mode, results in selection of a boot device storing the boot code nub, and if the apparatus is in a default encoded chip select mode, results in selection of a boot device storing the boot code nub.

William discloses a method and apparatus to provide chip selects in either encoded or unencoded words to address any memory devices. William discloses a

computer system (corresponding to the claim's apparatus) comprising a controller (William's Fig 1: #12 subsystem controller). William's controller further comprises address translation elements (William's Fig 4, TLB table, address decode logic, chip select logic) that capable of providing the address lines and chip select lines to address any memory devices. According to William's method, the chip select word can be either an unencoded chip selects word (William's Fig 3, CS: bits 8-1), or encoded chip select word (William's Fig 3: CS bits 2-0). Both unencoded chip select word and encoded chip select word select the same memory device, for example, in Fig 3, values "00000010" and "001" points to the same memory device (William's column 6, lines 33-50). William clearly teaches the need to quickly provide addresses, and chip select signals to memory devices and thereby improve the performance of the overall system. In this instance, William teaches a novel approach that is the controller itself with its associating logic can quickly handle chip select values in both encoded and unencode forms and quickly provide individual chip select lines to memory devices (William's column 1 lines 37-46, column 2 lines 6-15, column 2, lines 20-25 quick providing of chip select signal to memory device reduce the overall time to select data in a row of memory device). Although William does not expressly discloses that the memory device stores the code to initializing the system. However, it's well known in the art that memory devices are used to stored variety of codes including boot code, initializing code, operating system code, application code. Thus William's controller clearly suggest to provide quick chip select lines to any memory devices in any period of time and thereby further improve the performance of the overall system. Regarding the boot code nub aspect of the claim. As discussed in the rationale of claim 24, the BIOS code comprises several information

modules, including the information module to configure the system such as chip selection mode being used in the system (corresponding to the claim's boot nub code), which must be stored in the first boot device, and loaded into the system first before loading other information modules such as the operating system.

As in claim 42, the claim recites executing the boot code nub, and in response to executing the boot code nub, updating one of the default unencoded chip select mode and the default encoded chip select mode to one of an unencoded chip select mode and an encoded chip select mode. Examiner notes that the claim can be understood as followings, in response to executing the boot code nub, the mode of the chip select is not changed. The claim rejected based on the same rationale as of claim 41. William's column 6 lines 1-5 further disclose the controller can be configured to operate in any encoding schemes.

Claim 43 rejected based on the same rationale of claim 33.

Claim 44 rejected based on the same rationale of claim 31.

Claim 45 rejected based on the same rationale of claim 35.

Claim 46 rejected based on the same rationale of claim 36.

Claim 47 rejected based on the same rationale of claim 38.

Claim 48 rejected based on the same rationale of claim 35.

Allowable Subject Matter

Claims 34,49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

As to the remarks filed on 2/2/07 on pages 11-14,

A) Examiner maintains that William teaches the claim's limitation of "..before controller initialization in response to a power up or a soft reset of the apparatus, configured to generate.." either an encoded chip select or an unencoded chip select as follows:

William further discloses the chip select is provided by using either the encoded chip select or the unencoded chip select (see William's Fig 3, column 5 line 59 to column 6 line 7, various encoded schemes can be implemented). Thus obviously, the choice of encoding chip select or unencoding chip select is configured by setting a value into a "mode" register in the controller (for example, the mode register configured/setting with value 0 for selecting the unencoding chip select, and the mode register configured/setting with value 1 for selecting the encoded chip select, William's column 5 lines 49-52 discloses several configuration registers for such configuration information in the system). At power up time, the registers in the system are cleared such that the system starts with an initial state. The registers are cleared for example, by well-known

mechanism in the art, using the reset signal at the power-up time. Thus the "mode" register is cleared (by reset signal) with value zero, **before** the BIOS code is read, to select the unencoded chip select and therefore configured to generate the unencoded chip select **before** the BIOS code is read in from a non-volatile device and initializing the controller or the system.

B) Regarding the Applicant's remarks on page 13 second paragraph, William clearly discloses the circuitry of the controller to perform the encoded generating an encoded and unencoded chip select as disclosed in William's Fig 3.

C) Examiner respectfully disagrees with the Applicant argument that somehow it would be detriment to add functionality into BIOS code.

The BIOS code as known in the art comprises several modules of information representing critical commands/data such as system configuration information, operating code for the system, being stored in storage elements of non-volatile memory devices. The BIOS code is loaded into the system and executing in a bootstrap manner. For example, the first information module stored in a first boot device having the configuration information for the system must be loaded first, before loading other information modules such as operating system. Thus it's obviously that the configuration information that indicates the state of the system, such as chip selection mode being used in the system, must be maintained in the non-volatile device, such as the first boot device, and loaded into the system before loading other information modules such as operating system.

Because BIOS code is organized into modules of information and loaded into the system in bootstrapping manner, therefore the configuration information, such as the

configuring to select encoded chip select or unencoded chip select can be stored in the first boot device and quickly loaded into the system.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

3-30-07